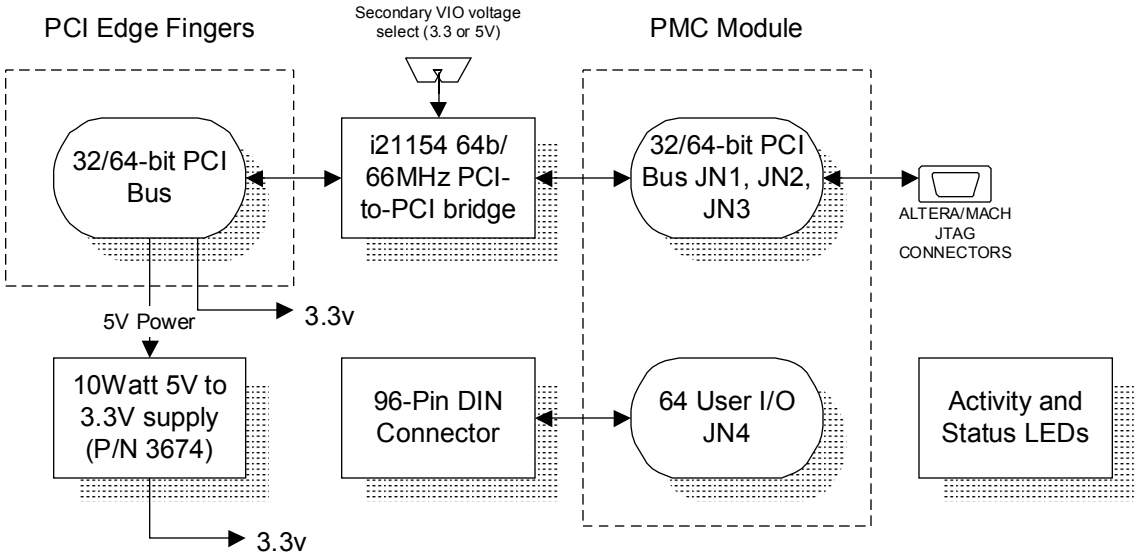
Bridged 64-bit/66MHz PMC-to-PCI adapter w/Fan Assy



This 64-bit PMC-to-PCI Adapter with PCI-to-PCI bridge permits delivery of PMC-derived applications in a standard PCI environment.

This product features a 21154 PCI-to-PCI bridge chip to assure PCI bus signal integrity even with multiple adapters plugged into a single PCI bus segment. The 21154 bridge will operate either at 33 MHz or 66 MHz PCI bus clock on either the primary or secondary side of the bridge. Dissimilar clock frequencies of 66 MHz primary side and 33 MHz secondary side works, but the 21154 does not support 33MHz on the primary side with 66 MHz on the secondary side. Any mix of 32 bit and 64 bit on the primary/secondary side is accommodated.

A 3.3V switching DC-to-DC converter is provided as a population option (order P/N 3674) on the board converts the 5V power from the PCI edge finger to 3.3V to the PMC. This allows operation in motherboards that do not support 3.3V power. The maximum current from the regulator is 3 Amps at 3.3 Volts. The other population option, P/N 3673, does not provide the DC-to-DC converter but takes 3.3V power directly from the PCI edge fingers.

Several LEDs visible from the edge of the board monitor power (PVIO, SVIO, +12V, -12V, 5V, 3.3V) and key PCI bus signals (INTx, BUSMODE1, REQ32). Two LEDs sense the VIO signal voltage to indicate if the slot uses 3.3V (VIO = 3.3V) or 5V (VIO = 5V) PCI bus signaling. These two LEDs – PVIO and SVIO – indicate voltage for the primary side and secondary side PCI bus, respectively.

An optional fan assembly (P/N 3675) is available that fits over two PMC-to-PCI adapter boards and provides substantial forced-air cooling of high-power PMC modules.

The BUSMODE[4..2] inputs to the PMC is set to 001 indicating use of the PCI bus for the PMC connectors.

The user may select either 3.3V or 5V secondary PCI bus signaling levels using a jumper on the PMC to PCI adapter board. The 3.3V / 5V signaling level for the primary PCI bus is established by the “VIO” power rail on the PCI bus edge finger.

The JTAG signals going to the PMC are brought out to 10-pin headers to allow users to program their PLD and FPGA logic on the PMC card. One header is configured for ALTERA use, the other for MACH PLD use.

The A and C rows of a 96-pin DIN connector, located toward the rear of the board, connect with the 64-pin user I/O connector (J4/P4) on the mezzanine card. This connection is specified by IEEE 1386 for the P2 connector on VMEbus boards and permits internal connection of rear I/O, should the PMC board support rear I/O connectivity.

A high quality 2.5 mm thick, machined aluminum panel, with a 0.5 mm chamfered edge, is provided on the PCI board bracket. This mimics the mechanics of a PMC installed on a VMEbus board or other host environments and allows the PMC bezel to be firmly positioned on the board.

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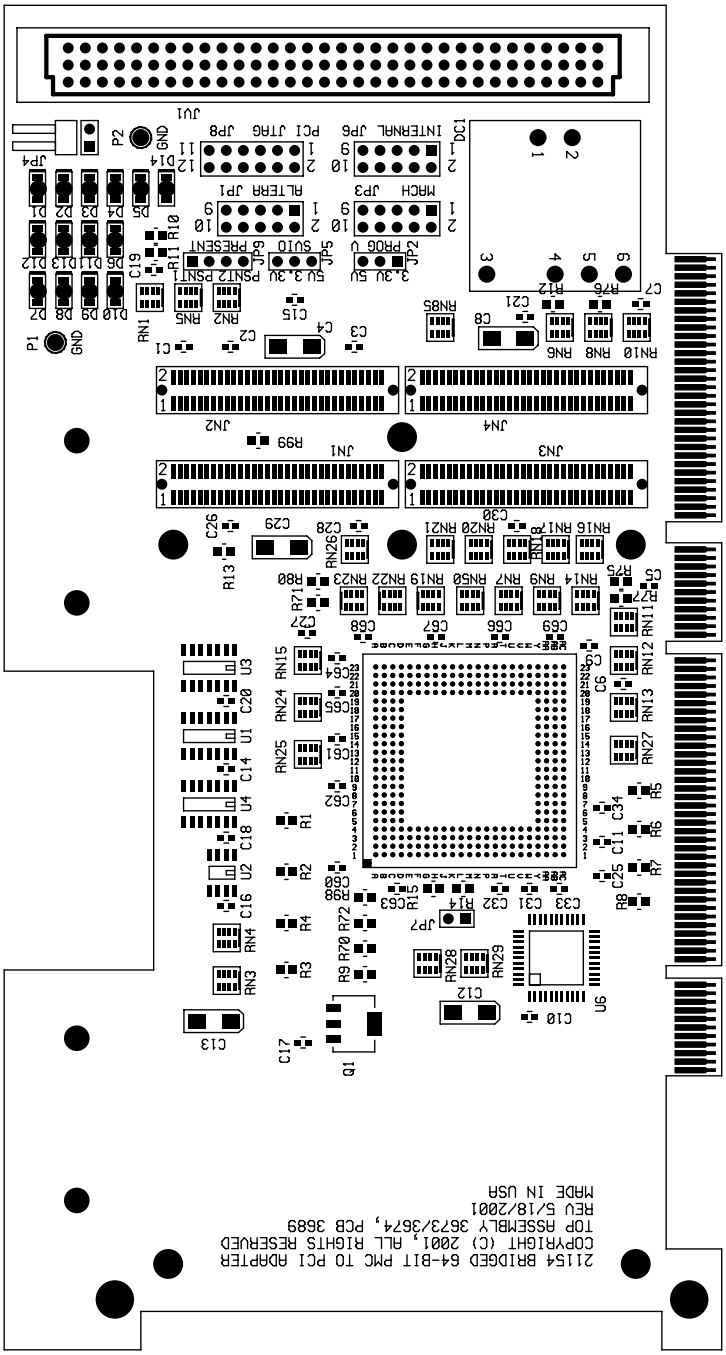

Product Summary

Technobox Part Numbers:	3673: Adapter with ***no*** 3.3V DC-to-DC converter (3.3V power comes from PCI bus)
	3674: Adapter with 3.3V DC-to-DC converter (only 5V PCI bus power is used to create 3.3V power)
	3675: Fan assembly (buy one for each two 3673/3674 board)
PCI Signaling Environment:	3.3V, 5V; 33 or 66 MHz; 32 or 64-bit