Digital I/O PMC

Conduction-Cooled 32-Channel RS485/422 Differential PMC

The Conduction-Cooled 32-channel Reconfigurable RS422/RS485 Digital I/O PMC provides a vehicle for implementing complex user-specific digital designs requiring a differential interface. Thirty-two (32) general-purpose RS422/RS485 driven digital I/O differential pairs are wired to the rear PN4 connector. For each of the 32 channels, the bidirectionality is controlled by an output from the FPGA.

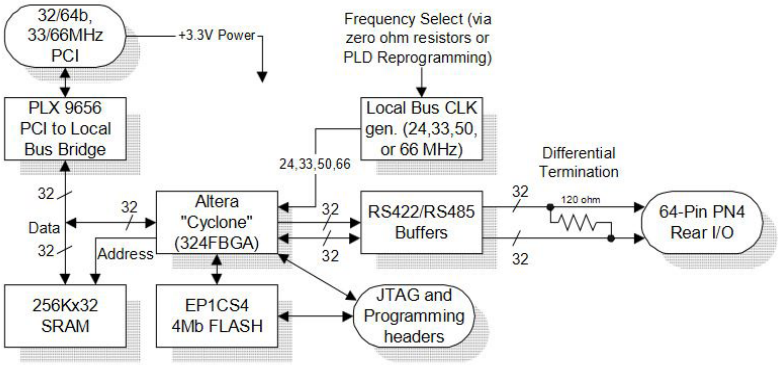
This product is a conduction-cooled version of the P/N4289 board. All features of the 4289 are retained, except the ICS1522 PLL has been eliminated in favor of using the Cyclone internal PLLs and the differential I/O is available at PN4 only. Also, the board is powered from the host strictly by the 3.3V supply while the original 4289 was powered strictly by the 5V. The host must now support 3.3V power to the PMC, 5V power is no longer needed.

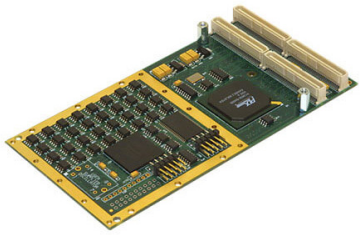
This product is ruggedized by using Industrial Temperature Range parts (-40 to +85 deg C) throughout and also by incorporating VITA 20 "Conduction-Cooled" PMC features. Additional "anti-fretting" holes per a recent revision of the VITA 20 standard are available as well as the secondary thermal interfaces for heat conduction. SN65HVD10QD RS485 chips are used with an upper operational temperature of +125 degrees C. Finally, the board is conformally-coated as a standard feature.

The product uses an Altera "Cyclone" FPGA in a 324 Fine-Line FPGA. This package spans the 4K, 12K and 20K logic element parts. The standard, stocked product uses an EP1C12F324I7 density/speed part (with12K LEs). For ease of migration, the Cyclone BGA pinout is the same as on the 4289 board.

Each of the 32 differential pairs is terminated with a 120ohm parallel resistance or an R/C termination as shown in the block diagram. Individual resistors are used with each differential pair, allowing for easy removal or value change on a per-channel basis.

With the proper FPGA design the 256K x 32b SRAM provided on the PMC is accessible from the Altera part as well as the PCI interface. The 32-bit data bus is shared between the ALTERA and the PCI interface devices. The SRAM address is driven by ALTERA outputs. This





4792

- **Provides 32 Channels of General-Purpose RS485/422 Digital I/O**
- **Supports 64-bit/66 MHz PCI Bus**
- **50K Logic Elements (9136 Populated w/ Intel 5CGXFC4C6F23I7N)**
- **Reprogrammable by Host, On-board Flash or USB Blaster Cable**
- **Local Bus SRAM (256K x 32-bit)**
- **Optional Header for Logic Analyzer Attachment**
- **Sample FPGA Design & Host "C" Code**
- **RoHS-compatible**
- **Lead-free**

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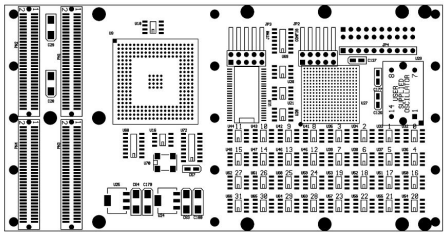
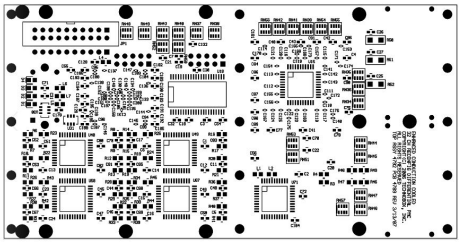


COMPONENT PLACEMENT VIEW - SIDE #1



COMPONENT PLACEMENT VIEW - SIDE #2

technique allows a variety of memory architectures for the SRAM: single-port SRAM, dual-port SRAM, one or more FIFOs, and even linked list structures for more complex applications.

The PLX local bus clock is selectable as 24 (default),33, 50, or 66 MHz using resistor-jumpers. Alternately, an ALTERA PLD on the board can be reprogrammed to provide virtually any local bus clock.

On power up, the Altera FPGA configuration cells are automatically loaded from a serial EPROM located onthe PMC. The user may override this default configuration by dynamically reprogramming the FPGA from the host processor, or by in-circuit burning of the reprogrammable FLASH EP1CS4 chip with the user's application. Two 10-pin headers are provided for development with ByteBlaster cables - one for the JTAG connection and the other for programming the EP1CS4.

An example implementation of a digital I/O board with dual-port access to the SRAM and corresponding "C"source code running in the host is provided with the product. QUARTUS development software is available directly from Altera.

SPECIFICATIONS

Typical Power Dissipation: TBD

Power Supplies Required: +3.3V Only

PCI Signaling Environment: 5V or 3.3V, 32/64b, 33/66MHz

ORDERING INFORMATION

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