

# PMC Carrier / Adapter

## 32/64 bit 33/66 MHz PCI-X to PMC-X Adapter

The PCI-X to PMC-X Adapter permits operation of a standard 32 or 64 bit PCI-X card in a PMC-X slot. It provides a migration path for PCI-X board suppliers to port their products to a PMC-X form factor. As the PMC-X equivalent board is developed, software development and migration can proceed with the original PCI-X board operating in a PMC-X environment. Also, developers can evaluate product performance in a PMC-X environment before committing to a PMC-X conversion effort.

This is a passive adapter (no PCI-to-PCI bridge chip) that requires no software setup. However, note that the PCI bus signaling level (3.3 or 5V) must match between the host PMC site and the PCI board. Also, for proper operation, 64-bit PCI cards must be used in a 64-bit capable PMC site.

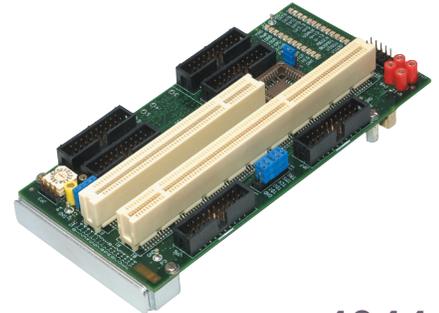
This board, which is the successor product to the popular P/N 1505 board, supports the new "PCI-X Capable" signal so that either legacy style PCI boards (33 or 66 MHz, 5V or 3.3V) or the newer PCI-X boards (up to 110MHz, 3.3V) can be used.

PMC-X connectors supporting 64 bit PCI bus are provided (PN1, PN2, PN3). One PCI-X edge finger connector supports keying for 32-bit 5V signaling PCI cards. A second edge finger connector supports keying for 32-bit or 64-bit 3.3V signaling PCI-X cards. A "universal" 5V/3.3V signaling PCI-X card can be used in either position.

The position of the PCI-X connector permits a standard short-length PCI-X board to be installed without interfering with the VME, cPCI backplane, or board front panel.

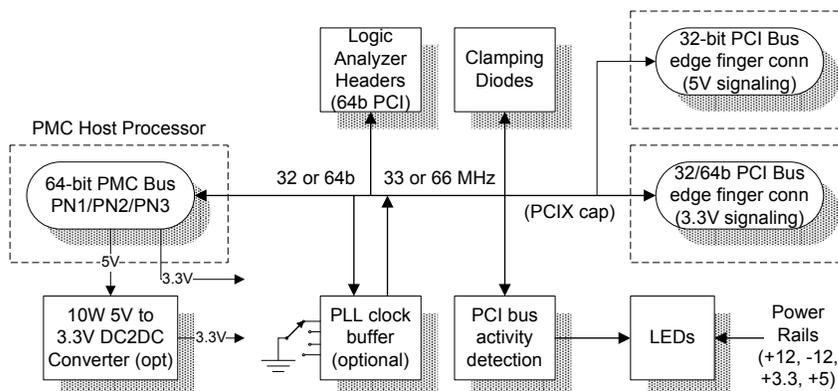
High-speed Schottky diodes clamp PCI-X signals to ground near the PCI-X connector. This practice minimizes signal undershoot and other transmission line effects. Furthermore, the board is an 8-layer impedance-controlled design, with 4 power plane and 4 signal planes. This design enhances signal quality to assure best possible success in using the product with high-speed PCI-X bus boards.

A user-installed Phase Lock Loop option may be ordered (P/N 4051)

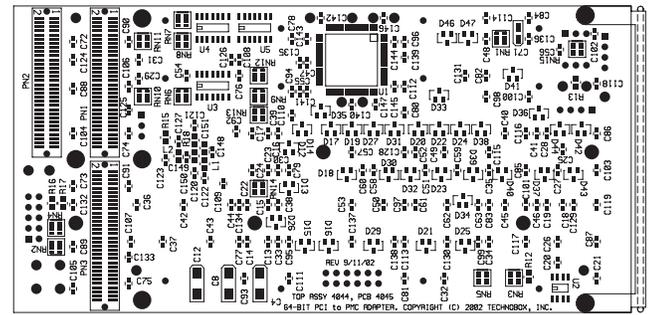
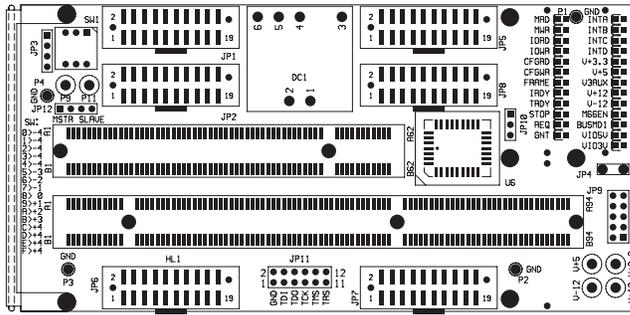


4044

- Supports PCI-X and Legacy PCI Cards
- Accepts 32- and 64-bit boards (33 or 66 MHz)
- Six 20-pin Headers for Analyzer Interface
- Special Circuit Measures Bus Utilization
- 8-layer Design Optimizes PCI-X Performance
- Optional PLL Clock Buffer Upgrade Package
- Optional 5V to 3.3V DC:DC converter



Technobox



to buffer the PCI clock. The circuit allows positioning of the PCI clock edge +/-4 ns from the nominal position in 1 ns steps using a rotary switch on the board. This allows “tweaking” of the PCI clock to optimize setup and hold times on the PCI-X bus. The PLL operates up to 110 MHz.

Six 20-pin box connectors permit Logic Analyzer visibility of the full

64-bit PCI-X bus. These connectors support HP 01650-63203 termination adapters.

LEDs monitor power supplies and key signals from the PCI-X bus. Logic provided on the board decodes the PCI-X bus cycles into Memory RD/WR, I/O RD/WR, and Configuration space RD/WR LED indicators. Pulse-stretchers allow visible detection of short-lived events. A novel

analog circuit provides a voltage (0 to 1 VDC) proportional to the bandwidth utilization of the PCI bus.

A factory-installed optional 10 Watt 5V to 3.3V DC to DC converter is available for those host systems that don't supply 3.3V power rail. Order P/N 4044 without the converter, and P/N 4068 with the converter installed.

### Specifications

- Temperature (Operating): 0 to 55 C
- Temperature (Storage): -40 to +85 C
- Altitude: Not specified or characterized (Typical similar equipment is at 15,000 ft.)
- Humidity (Operating/Storage): 5% to 90% non-condensing
- Vibration: Not specified or Characterized
- MTBF: Can be provided upon request
- Typical Power Dissipation: TBD
- Power Supplies Required: 5V, 3.3V + PCI board requirements
- PCI Environment: 5 Volt or 3.3V, 33 or 66 MHz, PCI or PCI-X

### Ordering Information

- 4044: No 5V to 3.3V DC:DC converter
- 4051: PLL Clock Buffer Upgrade Package
- 4068: With 5V to 3.3V DC:DC converter

