Digital I/O XMC

Advanced 32-Channel RS485/422 Differential XMC

The conduction-cooled Technobox, Inc. P/N 8643 Advanced 32-channel RS485/422 XMC is a third generation successor to our PMC solutions 2674 and 4289, both having been in continuous production since their introduction in the late 1990s. Whereas the 2674 and 4289 offered 4K and 12K Logic Elements (LEs) respectively, the 8643 provides the approximate equivalent of 50K LEs within its Intel® Cyclone® V GX FPGA (5CGXFC4C6F2717N). The Cyclone V also provides considerably more internal SRAM and several PLLs, as well as multipliers that are typically used for DSP applications.

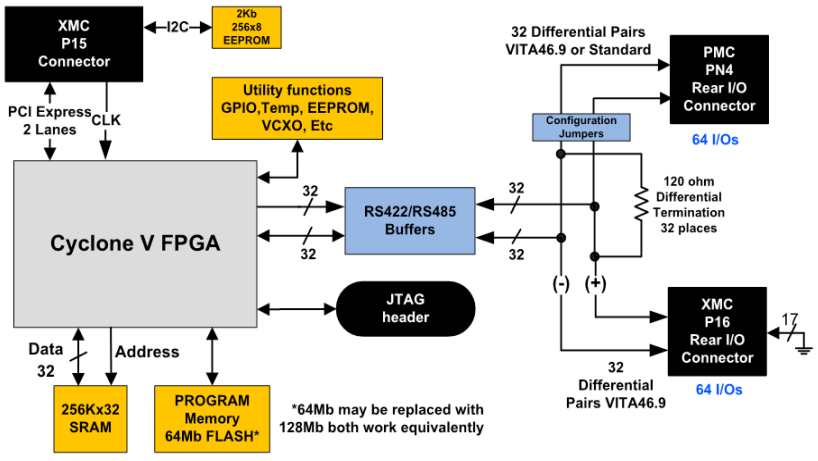
Many key features of the 2674/4289 designs are retained such as asynchronous SRAM, 32 RS485 differential pairs, the facility to download FPGA code via PCI/PCI Express®, a local sensor to monitor board temperature, and JTAG programming via an Altera USB-Blaster™. Also carried over are FPGA-driven user LEDs, silicon delay lines for critical asynchronous FPGA circuits, serial EEPROM for user data, and an option for a precision oscillator.

The 8643 conduction-cooling features along with the PN4 and/or P16 rear IO connectors differentiate it from the air-cooled 7757.

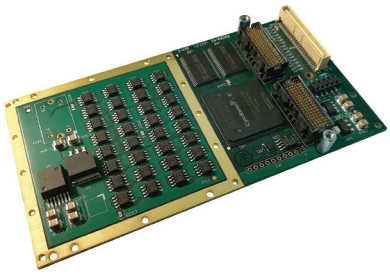
The 8643 FPGA and IO circuitry is identical to 7757 so FPGA designs and code from 7757 projects will run on the 8643 without modification and vice versa.

The 8643 supports up to two GEN-1 (2.5 Gb/s) PCI Express lanes to a host processor via its P15 connector (either VITA 42 or VITA 61 style). Furthermore, the PCIe interface is built into the Intel Cyclone V GX as a hard-core block, greatly simplifying access to PCIe resources.

FPGA design programming is performed using Intel's Quartus® FPGA design software tools. A free web edition is available from Intel. Technobox, Inc. provides sample FPGA and C code as a foundation for end user designs. Generally, designers will use Intel's Qsys to implement internal FPGA buses for hooking up the PCIe core to user application blocks.



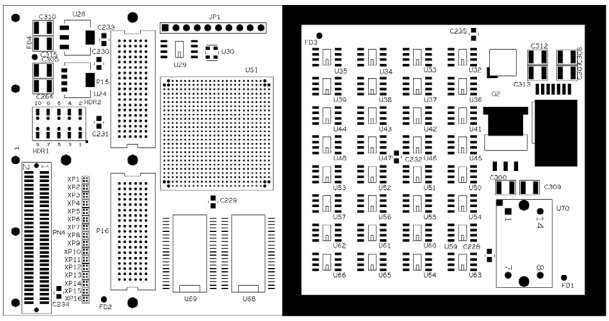
BLOCK DIAGRAM



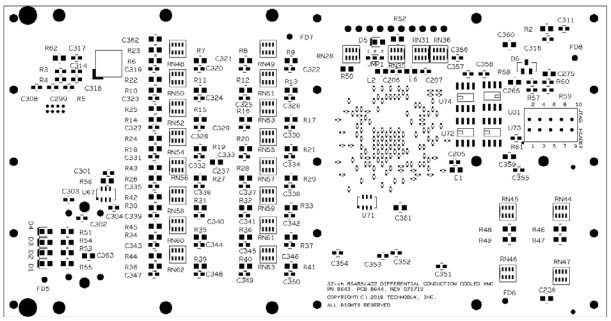
8643

- **FPGA-based, 32-Channel General-purpose Digital I/O XMC (VITA 42 or VITA 61)**
- **Altera® Cyclone® V architecture (5CGXFC4C6 standard population)**
- **Rear I/O via PN4 connector**
- **Rear I/O via P16 connector**
- **Conduction-cooled VITA 20**
- **External SRAM (256k x 32b)**
- **GEN-1 PCIe®, 2 lanes (2.5 Gb/s each); CvP mode limits operation to 1 lane**
- **Programmable from host via PCIe, on-board Flash, or direct via Altera USB Blaster**
- **User defined LEDs**
- **User accessible temp sensor**
- **Silicon delay lines**
- **Serial EEPROM**
- **Flexible termination scheme**
- **Separate direction control for each RS485 channel**
- **Sample FPGA design and host C code**
- **Industrial temperature design**
- **RoHS-compatible, Lead-free**

Technobox®, inc.



COMPONENT PLACEMENT VIEW - SIDE #1



COMPONENT PLACEMENT VIEW - SIDE #2

Three configuration options can be used to load a design into the Cyclone V FPGA. The first method is downloading code using Intel's Configuration via Protocol (CvP) over a single lane, an arrangement that allows configuring of the FPGA via the PCIe interface. In this case, an initial ring design is loaded from on-board FLASH memory, affording the FPGA some fundamental PCIe access. Subsequently, the host can load application code to the FPGA. (NOTE: CvP restricts operation of the 8643 to a single lane.) Using the second initialization method, application code is transferred from FLASH memory to the FPGA on power up. A third method can be used to initialize the 8643 directly via a cable connection to a USB Blaster.

Both types of rear I/O interfaces, PN4 and P16, support thirty-two (32) RS485/422 differential pairs (64 signals) from an array of 65LHV10 transceivers, each able to support rates up to 25 Mb/s. Directionality of each pair is controlled by a separate signal from the FPGA. Termination is 120 ohms parallel. R/C termination with failsafe biasing can be used as a population option to accommodate specific end-user termination requirements.

The base part number, 8643, for this family of XMCs is configured: with P16, PN4 and VITA 42 connectors installed & with PN4 set for VITA 46.9 differential pairing. For changes to the base part number, a unique part numbers will be assigned when ordered.

SPECIFICATIONS

Temperature (Operating): -40 to +85 degrees C

Temperature (Storage): -55 to +105 degrees C

Altitude: Not specified or characterized - similar equip. is at 15,000 ft.

Humidity (Operating/Storage): 5% to 95% non-condensing.

Vibration: Not specified or characterized

Shock: Not specified or characterized

MTBF: Can be calculated upon request

PCI Express: 2-lane, Gen. 1

Voltages Required: +3.3V, VPWR (+5V or +12V)

Power: Application dependent

Size: 74 mm x 143.7 mm

ORDERING INFORMATION

8643: Advanced 32-Channel RS485/422 Differential XMC

8260: Reverse Compact XMC-to-PCI Express (PCIe) Adapter - 8X (J16/JN4 to 68-Pin Connector at Bracket)

7757: Advanced Reconfigurable 32-Channel RS485/RS422 Differential I/O FPGA-Based XMC (VITA 42)

Technobox®, inc.

 DS8643-B91106

Technobox, Inc.
154 Cooper Road, Suite 901
West Berlin, NJ 08091
Phone: 856-809-2306 • **Fax:** 856-809-2601
Email: sales@technobox.com
Website: www.technobox.com